REMARKS

In the non-final Office Action, the Examiner rejected claims 14, 16, 17, 22, 23, and 27 under 35 U.S.C. § 103(a) as unpatentable over Boesch et al. (U.S. Patent No. 6,188,877, hereinafter "BOESCH") in view of Ono et al. (U.S. Patent No. 7,139,538, hereinafter "ONO"); and rejected claims 14, 16, 17, and 19-29 under 35 U.S.C. § 103(a) as unpatentable over Adar (U.S. Patent No. 5,774,017, hereinafter "ADAR") in view of ONO.

By way of this Amendment, Applicants amend claims 14, 16, 17, 21-23, and 27 to improve form. Applicants traverse the Examiner's rejections under 35 U.S.C. § 102 in light of the amendments provided herein. Claims 14, 16, 17, and 19-29 remain pending.

REJECTION UNDER 35 U.S.C. § 103 BASED ON BOESCH AND ONO

In paragraph 3 of the Office Action, the Examiner rejected claims 14, 16, 17, 22, 23, and 27 under 35 U.S.C. § 103(a) as allegedly unpatentable over BOESCH and ONO. The rejection is respectfully traversed.

For example, independent claim 14 is directed to a method, of reducing a negative influence on signals transmitted in one of at least two frequency bands provided by a same cellular network, that comprises providing a first connection between a signal generating chip and a signal processing chip; providing a second connection between the signal generating chip and the signal processing chip; providing at least one switch connected to the first connection and the second connection and located between the signal generating chip and the signal processing chip; transmitting or receiving, by the signal generating chip, signals in a first frequency band, of the at least two frequency

bands provided by the same cellular network, on the first connection; transmitting or receiving, by the signal generating chip, signals in a second frequency band, of the at least two frequency bands provided by the same cellular network, on the second connection; when transmitting or receiving the signals in the first frequency band on the first connection, breaking, by the at least one switch, the second connection between the signal generating chip and the signal processing chip; and when transmitting or receiving the signals in the second frequency band on the second connection, breaking, by the at least one switch, the first connection between the signal generating chip and the signal processing chip.

BOESCH and ONO, whether taken alone or in any reasonable combination, do not disclose or suggest the combination of features recited in claim 14. For example, BOESCH and ONO do not disclose breaking a second connection between a signal generating chip and a signal processing chip when transmitting or receiving signals in a first frequency band on a first connection; and breaking the first connection between the signal generating chip and the signal processing chip when transmitting or receiving signals in a second frequency band on the second connection, where the breaking of the second connection and the breaking of the first connection are performed by at least one switch connected to the first connection and the second connection and located between the signal generating chip and the signal processing chip, as recited in claim 14.

The Examiner alleged that BOESCH discloses breaking the second connection and breaking the first connection, and admitted that BOESCH does not disclose or suggest a signal generating chip or a signal processing chip (Office Action, pages 5-6).

The Examiner alleged that ONO discloses a "generating circuit chip" and a "power amplifying chip" and relied upon an RF IC 110 as allegedly corresponding to the generating circuit chip and an RF power module 200 as allegedly corresponding to the power amplifying chip (Office Action, page 6). Without acquiescing in the Examiner's allegations, Applicants submit that BOESCH and ONO do not disclose or suggest breaking a second connection between a signal generating chip and a signal processing chip when transmitting or receiving signals in a first frequency band on a first connection; and breaking the first connection between the signal generating chip and the signal processing chip when transmitting or receiving signals in a second frequency band on the second connection, where the breaking of the second connection and the breaking of the first connection are performed by at least one switch connected to the first connection and the second connection and located between the signal generating chip and the signal processing chip, as recited in claim 14.

ONO discloses that RF IC 110 is a high-frequency signal processing circuit formed as a semiconductor integrated circuit having a modulating/demodulating circuit, band pass filters, and low-noise amplifiers (col. 4, lines 26-35). ONO discloses that RF module 200 includes a power amplifier 210a for amplifying a transmission signal of 900 MHz in the frequency band of the GSM and a power amplifier 210b for amplifying a transmission signal of 1800 MHz in the frequency band of the DCS (col. 4, lines 53-58). ONO discloses that components of RF module 200 are formed as semiconductor integrated circuits on multiple semiconductor chips (col. 9, lines 31-56).

Even assuming, for the sake of argument, that ONO discloses that RF IC 110 is located on one chip and reasonably corresponds to a signal generating chip, and that RF module 200 is located on another chip and reasonably corresponds to a signal processing chip (points that Applicants do not concede), ONO does not disclose at least one switch that is connected to first and second connections between the RF IC chip and the RF module chip and that is located between the RF IC chip and the RF module chip, as would be required by claim 14 based on this interpretation of ONO. Rather, ONO discloses that switches 420a and 420b are located in a front end module 400 located between the RF module 200 and the antenna (Figure 1; col. 4, lines 44-48; col. 5, lines 6-12). Thus, ONO does not disclose or suggest breaking a second connection between a signal generating chip and a signal processing chip when transmitting or receiving signals in a first frequency band on a first connection; and breaking the first connection between the signal generating chip and the signal processing chip when transmitting or receiving signals in a second frequency band on the second connection, where the breaking of the second connection and the breaking of the first connection are performed by at least one switch connected to the first connection and the second connection and located between the signal generating chip and the signal processing chip, as recited in claim 14.

BOESCH's figures illustrate several embodiments of an amplifier circuit. BOESCH does not disclose that the amplifier circuit is implemented in a chip. Nevertheless, even assuming, for the sake of argument, that it is reasonable to modify the BOESCH system to include the amplifier circuit on a chip (as allegedly disclosed by ONO), that a signal generating chip is the component generating the 1900 and 800 MHz

signals in BOESCH, that the 1900 MHz signal is provided via a first connection, and that the 800 MHz signal is provided via a second connection (points that Applicants do not concede), BOESCH does not disclose or suggest at least one switch that is connected to first and second connections between the amplifier circuit chip and the signal generating chip and that is located between the amplifier circuit chip and the signal generating chip, as would be required by claim 14 based on this interpretation of BOESCH.

For example, in the embodiment of Figure 4, BOESCH discloses a 1900 MHz RF input 405 and an 800 MHz RF input 415 to the amplifier circuit. Even with the assumptions above, BOESCH does not disclose or suggest at least one switch that is connected to the first and second connections between the amplifier circuit chip and the signal generating chip and that is located between the amplifier circuit chip and the signal generating chip. Rather, BOESCH discloses a switching network 418 that includes switches 422, 424, and 426 (Figure 4; col. 7, lines 15-20). BOESCH discloses that switching network 418 is part of the amplifier circuit (Figure 4). Thus, switching network 418, of BOESCH, is not connected to first and second connections between the amplifier circuit chip and the signal generating chip and is not located between the amplifier circuit chip and the signal generating chip. Thus, BOESCH, even if modified by ONO, does not disclose or suggest breaking a second connection between a signal generating chip and a signal processing chip when transmitting or receiving signals in a first frequency band on a first connection; and breaking the first connection between the signal generating chip and the signal processing chip when transmitting or receiving signals in a second frequency band on the second connection, where the breaking of the

second connection and the breaking of the first connection are performed by at least one switch connected to the first connection and the second connection and located between the signal generating chip and the signal processing chip, as recited in claim 14.

Similarly, with regard to Figure 7, BOESCH discloses a switching circuit 725 that is provided as part of the amplifier circuit (col. 10, lines 14-29). Thus, switching circuit 725, of BOESCH, is not connected to first and second connections between the amplifier circuit chip and the signal generating chip and is not located between the amplifier circuit chip and the signal generating chip. Thus, BOESCH, even if modified by ONO, does not disclose or suggest breaking a second connection between a signal generating chip and a signal processing chip when transmitting or receiving signals in a first frequency band on a first connection; and breaking the first connection between the signal generating chip and the signal processing chip when transmitting or receiving signals in a second frequency band on the second connection, where the breaking of the second connection and the breaking of the first connection are performed by at least one switch connected to the first connection and the second connection and located between the signal generating chip and the signal processing chip, as recited in claim 14.

For at least the foregoing reasons, Applicants respectfully submit that claim 14 is patentable over BOESCH and ONO, whether taken alone or in any reasonable combination.

Amended independent claims 16, 17, 22, 23, and 27 recite features similar to, yet possibly different in scope than, the features described above with regard to claim 14. Accordingly, claims 16, 17, 22, 23, and 27 are patentable over BOESCH and ONO,

whether taken alone or in any reasonable combination, for at least reasons similar to the reasons given with regard to claim 14.

Accordingly, Applicants respectfully request the Examiner's reconsideration and withdrawal of the rejection of claims 14, 16, 17, 22, 23, and 27 under 35 U.S.C. § 103 based on BOESCH and ONO.

REJECTION UNDER 35 U.S.C. § 103 BASED ON ADAR AND ONO

In paragraph 4 of the Office Action, the Examiner rejected claims 14, 16, 17, and 19-29 under 35 U.S.C. § 103(a) as allegedly unpatentable over ADAR and ONO. The rejection is respectfully traversed.

For example, independent claim 14 is directed to a method, of reducing a negative influence on signals transmitted in one of at least two frequency bands provided by a same cellular network, that comprises providing a first connection between a signal generating chip and a signal processing chip; providing a second connection between the signal generating chip and the signal processing chip; providing at least one switch connected to the first connection and the second connection and located between the signal generating chip and the signal processing chip; transmitting or receiving, by the signal generating chip, signals in a first frequency band, of the at least two frequency bands provided by the same cellular network, on the first connection; transmitting or receiving, by the signal generating chip, signals in a second frequency band, of the at least two frequency bands provided by the same cellular network, on the second connection; when transmitting or receiving the signals in the first frequency band on the first connection, breaking, by the at least one switch, the second connection between the

signal generating chip and the signal processing chip; and when transmitting or receiving the signals in the second frequency band on the second connection, breaking, by the at least one switch, the first connection between the signal generating chip and the signal processing chip.

ADAR and ONO, whether taken alone or in any reasonable combination, do not disclose or suggest the combination of features recited in claim 14. For example, ADAR and ONO do not disclose breaking a second connection between a signal generating chip and a signal processing chip when transmitting or receiving signals in a first frequency band on a first connection; and breaking the first connection between the signal generating chip and the signal processing chip when transmitting or receiving signals in a second frequency band on the second connection, where the breaking of the second connection and the breaking of the first connection are performed by at least one switch connected to the first connection and the second connection and located between the signal generating chip and the signal processing chip, as recited in claim 14.

The Examiner alleged that ADAR discloses breaking the second connection and breaking the first connection, and admitted that ADAR does not disclose or suggest a signal generating chip (Office Action, pages 6-7). The Examiner alleged that ONO discloses a "generating circuit chip" and a "power amplifying chip" and relied upon RF IC 110 as allegedly corresponding to the generating circuit chip and RF power module 200 as allegedly corresponding to the power amplifying chip (Office Action, page 7). Without acquiescing in the Examiner's allegations, Applicants submit that ADAR and ONO do not disclose or suggest breaking a second connection between a signal

generating chip and a signal processing chip when transmitting or receiving signals in a first frequency band on a first connection; and breaking the first connection between the signal generating chip and the signal processing chip when transmitting or receiving signals in a second frequency band on the second connection, where the breaking of the second connection and the breaking of the first connection are performed by at least one switch connected to the first connection and the second connection and located between the signal generating chip and the signal processing chip, as recited in claim 14.

ONO discloses that RF IC 110 is a high-frequency signal processing circuit formed as a semiconductor integrated circuit having a modulating/demodulating circuit, band pass filters, and low-noise amplifiers (col. 4, lines 26-35). ONO discloses that RF module 200 includes a power amplifier 210a for amplifying a transmission signal of 900 MHz in the frequency band of the GSM and a power amplifier 210b for amplifying a transmission signal of 1800 MHz in the frequency band of the DCS (col. 4, lines 53-58). ONO discloses that components of RF module 200 are formed as semiconductor integrated circuits on multiple semiconductor chips (col. 9, lines 31-56).

Even assuming, for the sake of argument, that ONO discloses that RF IC 110 is located on one chip and reasonably corresponds to a signal generating chip, and that RF module 200 is located on another chip reasonably corresponds to a signal processing chip (points that Applicants do not concede), ONO does not disclose at least one switch that is connected to first and second connections between the RF IC chip and the RF module chip and that is located between the RF IC chip and the RF module chip, as would be required by claim 14 based on this interpretation of ONO. Rather, ONO discloses that

switches 420a and 420b are located in a front end module 400 located between the RF module 200 and the antenna (Figure 1; col. 4, lines 44-48; col. 5, lines 6-12). Thus, ONO does not disclose or suggest breaking a second connection between a signal generating chip and a signal processing chip when transmitting or receiving signals in a first frequency band on a first connection; and breaking the first connection between the signal generating chip and the signal processing chip when transmitting or receiving signals in a second frequency band on the second connection, where the breaking of the second connection and the breaking of the first connection are performed by at least one switch connected to the first connection and the second connection and located between the signal generating chip and the signal processing chip, as recited in claim 14.

ADAR's figures illustrate several embodiments of an amplifying apparatus. With regard to Figure 8, ADAR discloses that the amplifying apparatus includes a GaAs MMIC power amplifier chip 302. ADAR does not specifically disclose that the amplifying apparatus or power amplifier chip 302 is connected to a signal generating chip via first and second connections. In the embodiment of Figure 8, ADAR discloses an 800 MHz input terminal 322 and a 1900 MHz input terminal 324. Even assuming, for the sake of argument, that it is reasonable to interpret the disclosure of ADAR as disclosing a signal generating chip as the component generating the 800 MHz signal and the 1900 MHz signal, that 800 MHz input terminal 322 is provided via a first connection, and that 1900 MHz input terminal 324 is provided via a second connection (points that Applicants do not concede), ADAR does not disclose or suggest at least one switch that is connected to the first and second connections between the power amplifier chip and the signal

generating chip and that is located between the power amplifier chip and the signal generating chip. Rather, ADAR discloses a switch 316 that is provided as part of power amplifier chip 302 (Figure 8; col. 12, line 66 – col. 13, line 11). Thus, switch 316, of ADAR, is not located between the signal generating chip and the power amplifier chip and, therefore, cannot break a first connection provided between the signal generating chip and the power amplifier chip, or a second connection provided between the signal generating chip and the power amplifier chip, as would be required by claim 14 based on this interpretation of ADAR. Thus, ADAR, even if modified by ONO, does not disclose or suggest breaking a second connection between a signal generating chip and a signal processing chip when transmitting or receiving signals in a first frequency band on a first connection; and breaking the first connection between the signal generating chip and the signal processing chip when transmitting or receiving signals in a second frequency band on the second connection, where the breaking of the second connection and the breaking of the first connection are performed by at least one switch connected to the first connection and the second connection and located between the signal generating chip and the signal processing chip, as recited in claim 14.

Similarly, with regard to Figure 5A, BOESCH discloses switches 190 and 192 that are provided as part of the amplifier circuit (col. 9, lines 57-62). Thus, switches 190 and 192, of BOESCH, are not connected to first and second connections between the amplifier circuit chip and the signal generating chip and are not located between the amplifier circuit chip and the signal generating chip. Thus, BOESCH, even if modified by ONO, does not disclose or suggest breaking a second connection between a signal

generating chip and a signal processing chip when transmitting or receiving signals in a first frequency band on a first connection; and breaking the first connection between the signal generating chip and the signal processing chip when transmitting or receiving signals in a second frequency band on the second connection, where the breaking of the second connection and the breaking of the first connection are performed by at least one switch connected to the first connection and the second connection and located between the signal generating chip and the signal processing chip, as recited in claim 14.

Similarly, with regard to Figure 4, BOESCH discloses a switch 158 that is provided as part of the amplifier circuit (col. 8, lines 31-38). Thus, switch 158, of BOESCH, is not connected to first and second connections between the amplifier circuit chip and the signal generating chip and is not located between the amplifier circuit chip and the signal generating chip. Thus, BOESCH, even if modified by ONO, does not disclose or suggest breaking a second connection between a signal generating chip and a signal processing chip when transmitting or receiving signals in a first frequency band on a first connection; and breaking the first connection between the signal generating chip and the signal processing chip when transmitting or receiving signals in a second frequency band on the second connection, where the breaking of the second connection and the breaking of the first connection are performed by at least one switch connected to the first connection and the second connection and located between the signal generating chip and the signal processing chip, as recited in claim 14.

For at least the foregoing reasons, Applicants respectfully submit that claim 14 is patentable over ADAR and ONO, whether taken alone or in any reasonable combination.

Claim 28 depends from claim 14 and is, therefore, patentable over ADAR and ONO for at least the reasons given with regard to claim 14.

Independent claims 16, 17, 22, 23, and 27 recite features similar to, yet possibly different in scope than, features described above with regard to claim 14. Accordingly, claims 16, 17, 22, 23, and 27 are patentable over ADAR and ONO, whether taken alone or in any reasonable combination, for at least reasons similar to the reasons given with regard to claim 14.

Claims 19-21 and 29 depend from claim 17, and claims 24-26 depend from claim 23. Without acquiescing in the Examiner's rejection of claims 19-21, 24-26, and 29, Applicants submit that claims 19-21, 24-26, and 29 are patentable over ADAR and ONO for at least the reasons given with regard to claims 17 and 23.

Accordingly, Applicants respectfully request the Examiner's reconsideration and withdrawal of the rejection of claims 14, 16, 17, and 19-29 under 35 U.S.C. § 103 based on ADAR and ONO.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants respectfully request the Examiner's reconsideration of the application and the timely allowance of the pending claims.

As Applicants' remarks with respect to the Examiner's rejections overcome the rejections, Applicants' silence as to certain assertions by the Examiner in the Office Action or certain requirements that may be applicable to such assertions (e.g., whether a reference constitutes prior art, reasons for modifying a reference and/or combining

references, assertions as to dependent claims, etc.) is not a concession by Applicants that such assertions are accurate or such requirements have been met, and Applicants reserve the right to dispute these assertions/requirements in the future.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue that remains unresolved, or should any new issues arise which could be eliminated through a discussion with Applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order to expedite further prosecution of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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